

System Specifications Continued

Active Memory: The amount of installed memory that is active can be programmably truncated in 1k sample increments/ch when shorter record lengths are needed. All channels have the same record length.

Organization: Programmable in 1k sample blocks between pre- and post-event memory segments for transient recording. All channels have the same segmentation, and pre and post trigger ratios.

Battery Backup: Digitized data stored in memory can be protected against power interruptions by connecting an external UPS such as the DSPT Model TRAPS-BP to the VXI +5V STDBY bus. 80mA @ 5V is required for each VX2805 module.

Type: Dynamic RAM.

CALIBRATION

Bridge Voltage Insertion: A precision 10kΩ resistor can be connected to either signal arm of the bridge and is driven by a 16-bit programmable bi-polar voltage source. Current flows of different values are injected into either side of the bridge to simulate multiple shunt resistors. This Digital Transducer Calibrator provides a high resolution, multi-point calibration.

Shunt Calibration: Accomplished with SIPS.

Gain Calibration: Internal multiple precision voltage references are used by the Model VX2805 processor and firmware to report gain set with 0.1% accuracy.

Programmable Internal Reference: 16-bit DAC for multi-point validation of dc linearity.

External Calibration Source: Using NIST traceable source and Auto_Cert. routine, the VX2824 will verify internal flash calibration coefficients against source and store verification date.

FRONT PANEL CONTROLS

ADDR: Dual HEX encoded rotary switch for VXI Logical Address within short I/O (A16) space. Valid settings are 01 through FE.

FRONT PANEL LED INDICATORS

MASTER: Green LED. On if unit is configured at the Master in a data collection mode.

CONVERT: Blue LED. On if unit is digitizing or storing ADC data to internal data memory.

BUSY: Yellow LED. LED blinks when the host computer is accessing via the VXI bus.

FAIL: Red LED On if unit failed power-on reset diagnostics or if a condition exists that prevents correct unit operation. On for 5 sec. after system reset or power-up.

FRONT PANEL CONNECTORS

INPUTS: 2 each 15-pin "D".

OUTPUTS: Excitation Out, Excitation Sense, Shunt Cal., Analog Out, Ext. Cal In. Amplimite 50 pin.

CLK/TRIG IN: ADC reference clock and trigger input. Differential 4-pin LEMO connector.

CLK/TRIG OUT: ADC reference clock and internal trigger output. Differential 4-pin LEMO connector.

DIGITAL:

Inputs: TTL compatible single ended >1kΩ, or 100Ω balanced differential operation.*

Outputs: TTL compatible single ended 50Ω drive or 100Ω balanced differential operation.*

*In CE markets: Differential only.

Protection: Buffered ±15V clamp 1A for 2μs or 35 VDC.

ACCESSORIES

SIPS: Smart Interface Panel System.

PIPS: Passive Interface Panel System.

ENVIRONMENTAL

Operating Temperature: 0 to 30°C

Non-operating Temperature: -20 to 85°C

Non-condensing

PHYSICAL:

VXI, single width, "C" size.

Addressing: A16, D16/D32.

Logical Address: Set by front panel switches.

VXI Model VX2805

8 Channel Data Acquisition Module

Highlights

- 8 Channels Per Module
- Each Channel Includes Signal Conditioning, Filter, ADC and Memory
- 16-Bit Resolution
- High Dynamic Range
- Up to 5M Samples/s/ch
- Simultaneous Sampling
- Dual Ported Memory Access
- 1k Snapshot Data FIFO for Each Channel
- 2.3MHz 3dB Bandwidth
- Buffered Analog Output for Each Channel
- Overload Detection for Each Channel
- Excellent Ch-to-Ch Phase Match
- 16M Samples Storage per Channel
- Multi-Event Recording
- Computer Controlled Calibration
- Digital Signal Processors
- Digital Filters, Flat Passband, Sharp Cutoff
- Internal and External Triggering
- Pre- and Post-Trigger Recording
- Gated Mode
- Dual Clock Rate Data Recording
- Constant Voltage Excitation
- SIPS Communication Port
- Fully Programmable
- Memory Battery Backup Capability
- Single Width, C-size, VXI Module

Description

The Model VX2824 is a complete integrated 8 channel data recording VXI module. Each channel includes a bridge signal conditioner, a low pass filter, a 16-bit 5M samples/sec/ch ADC, and 16M samples of DRAM storage per channel.

Built-in signal conditioning is suitable for strain gauge bridge-type transducers and for voltage signals. Constant voltage excitation is independently programmable for each channel. Special function signal conditioning requirements can be accommodated with the SIPS (Smart Interface Panel System) product family and controlled by the VX2805 on-board processor.

Input full scale sensitivity is programmable from ±10mV to ±5V in 3dB steps. A 16-bit ADC provides high accuracy, a high dynamic range and resolutions from 340nV to 170μV per count. Offset correction range is ±2.5V with 16-bit resolution. A dedicated signal processor in each channel provides superb digital filtering. Filter F_{co} auto-tracks the sample rate, plus custom filter download capabilities. Dedicated hardware can generate a trigger from the analog signal being digitized on Channel #1 using either level and slope, or window criteria. Trigger Holdoff can be invoked to reject threshold crossings of short duration. Holdoff can improve triggering reliability under noisy signal conditions.

Heritage

The VX2805 is a fourth generation COTS product. The predecessors to this module, interfaced with IMPAX software (also COTS), have been used to accurately characterize initial dynamics for launch vehicles such as Titan, as the "turn-key" Lift Off Instrumentation System (LOIS), and Atlas, as the Lift Off Instrumentation System for Atlas (LISA). The VX2805 is being used in a prestigious shock laboratory for research and validation of state of the art accelerometers, and at the world's largest automotive air bag manufacturer, for the development and production testing of air bags.



Advanced Research Products
1010 Timothy Drive
San Jose, CA 95133
Telephone: 408.918.2500
Fax: 408.918.2580
email: adv_res@sd-star.com
www.spectraldynamics.com

For more information contact:
Mark Remelman, 510.252.0475, remelmanm@sd-star.com



Description Continued

The storage DRAM is initially available as 16M samples per channel, and allows for future expansion. It can be programmably configured for pre- and post-event data storage and can be programmably truncated. DRAM may be divided into 2, 4 or 8 segments for multiple event recording. Data stored in DRAM can be battery backed up using an external uninterruptable power source. The VX2805 auto bridge balance

function can be initiated by computer command. A complete end-to-end calibration of each channel, including the transducer, can be performed by a computer calibration routine using either switched in external calibration resistors or the unique internal shunt emulation circuit. The shunt emulation technique can provide a fast, multi-point calibration check without operator intervention.

System Specifications

SIGNAL INPUT

<i>Type:</i>	Differential Transducer Connection: 8 wires plus shield, 1,2 or 4 active bridge arms.
<i>Connector Type</i>	"D" style 15-pin.
<i>Input Impedance:</i>	2 M Ω differential, 1 M Ω to ground.
<i>Full Scale Ranges:</i>	$\pm 10\text{mV}$ to $\pm 5\text{V}$, programmable with 3dB ($\approx 50\%$) steps, 19 ranges.
<i>Accuracy After Autocalibration:</i>	$\pm 0.1\%$ of full scale $\pm 25\mu\text{V}$
<i>Gain Temp Coeff:</i>	$< 0.025\%/^{\circ}\text{C}$
<i>Offset Temp Coeff:</i>	$< 0.02\%/^{\circ}\text{C}$
<i>Linearity:</i>	$\pm 0.05\%$ of full scale.
<i>Bandwidth:</i>	dc - 1.1MHz $\pm 0.1\text{dB}$ at 2.5M sample/s. dc - 2.3MHz +0, -3dB at 5M sample/s.
<i>CMRR dc-100Hz:</i>	80dB $\pm 500\text{mV}$ to $\pm 5\text{V}$ 90dB for full scales $\leq \pm 500\text{mV}$
<i>CM Voltage Range:</i>	$\pm 10\text{V}$ including signal.
<i>Crosstalk:</i>	$> 90\text{dB}$ isolation ch-to-ch.
<i>Noise:</i>	20nV/rootHz + 4 counts RMS.
<i>Protection:</i>	Buffered $\pm 15\text{V}$ clamp Max 1A for 2 μs , 35V DC

ANALOG OUTPUT

An auxiliary analog output is available at the front panel from each channel. The level is $\pm 1\text{V}$ into 50 ohms for a \pm full scale signal.

FUNCTIONS

Offset Control: $\pm 2.5\text{V}$ 16 Bit resolution.

Offset Zero: An Autozero routine built in to the VX2805 will set the ADC output to zero using the Offset DACs. Autozero is intended for use with voltage type input signals. Autozero can be initiated by computer command.

Bridge Balance: When a bridge type transducer is used, an auto bridge balance routine controlled by the VX2805 processor will set the ADC output to zero using the 16-bit balance DAC. Range is $\pm 1\text{mA}$ times bridge resistance $\pm 10\text{mV}$. Auto Bridge Balance can be initiated by computer command.

OVERLOAD DETECTION

Automatic overload detection and reporting for each channel.

SOURCE SELECTION

Software controlled input selection is provided. Selections include external transducer, internal and external reference source, internal short to ground and \pm excitation voltage. A low thermal EMF relay selects between the signal and other inputs. The source for the calibration bus is then independently selectable as internal reference, short to ground or external calibration source.

EXCITATION

Constant Voltage: 0 to $\pm 10\text{V}$ (20V between the plus and minus excite terminals), programmable with 12-bit resolution. Over-current protection. After power up self test, excitation is nominally zero to protect connected transducers. All channels of excitation can be shut off by a single software command.

SIPS Drive: Used for constant current, constant voltage extended current drive capabilities.

ADC

Simultaneous Sampling: Individual 16-bit Sigma-Delta ADC per channel. An array of VX2805s can be configured for synchronized simultaneous sampling. Master/Slave clocking is accomplished via VXI local bus.

CLOCK

Internal: 5M to 1.25k samples/s/ch, programmable, with tracking filter. Clock step "1, 2, 5" style

External: Has phase-lock clock input and output ports for synchronization of multiple chassis of VX2824s.

DUAL CLOCK RATE DATA COLLECTION

During acquisition data may be sub-sampled at an integer sub-multiple from 0 to 256 to reduce data volume when high resolution is not required. Sub-sampling is controlled via the external trigger input connector. Tag RAM keeps track of transitions for correct readout indexing.

System Specifications Continued

GATED MODE FOR BURST RECORDING

When gate/trigger input is high, data is collected at specified rate. When gate signal is low, data collection is suspended. Tag RAM keeps track of transitions for correct readout indexing.

FILTERS

Description: The VX2805 uses 3 levels of filtering: analog, digital within the ADC, and digital within the signal processors. A sigma delta type ADC over samples the input signal by a factor of 8 times the maximum sample rate, then integrates and digitally filters the data. It is this over sampling rate that determines the aliasing frequency of the ADC, which is 20MHz. The ADC is preceded by an analog filter having 90dB attenuation at 20MHz.

The ADC has multiple FIR filters providing flat response to 1.01MHz and $> 85\text{dB}$ attenuation above 1.49MHz. The dc to 1MHz pass band ripple is $< 0.01\%$ of full scale at 2.5M sample/s. -3dB at 2.3MHz $> 82\text{dB}$ at 3.2MHz at 5M sample/s.

Dedicated signal processors reduce the ADC data to the required sampling rate and performs digital filtering which tracks that sampling rate.

Filter Characteristics:

Sample Rate	Pass band	Rejection band	Atten.
Sa/s	Hz	Hz	dB
5.0M	2.3M	3.2M	> 82
2.5M	1M	1.56M	85
1.25M	500k	780k	95
500k	200k	312k	95
250k	100k	156k	> 100
125k	50k	78k	> 100
50k	20k	31.2k	> 100
25k	10k	15.6k	> 100
12.5k	5k	7.8k	> 100
5k	2k	3.12k	> 100
2.5k	1k	1.56k	> 100
1.25k	500	780	> 100

TRIGGER

There are 4 stop trigger sources:

1 Software Trigger. The VX2805 can be triggered by a VME command.

2 Data Flow Trigger. The VX2805 can be triggered when the channel #1 ADC output (a 16-bit digital value) satisfies programmable 16-bit criteria; slope and level or amplitude window. *Level:* \pm full scale; *Slope:* Positive, Negative; *Window:* Trigger when the signal amplitude crosses upper or lower boundary of a window. Boundaries programmable to \pm full scale.

3 External Trigger. The VX2805 can be triggered by a TTL pulse received at the front panel Trig Input.

4 Real Time Trigger. The VX2805 can be triggered when the analog input signal on channel #1 reaches and remains at or above a programmable threshold for a programmable number of samples. *Threshold:* \pm full scale, 12-bit resolution.

Trigger Holdoff: When enabled, the signal must remain over threshold for a programmable number of 100ms time intervals (up to 255) to qualify as a trigger condition. Holdoff greatly reduces susceptibility to false triggers that could be caused by noise on the signal input line.

Trigger Output: Any of the trigger sources can also be programmed to produce a pulse or level at the front panel TRIG OUT connector to trigger an external device. There are 6 selectable trigger lines for group triggering.

System Triggering: A trigger pulse is also generated on the VXI Local Bus to simultaneously trigger multiple VX2805 modules.

Latching Mode: When enabled and triggered, the latching mode will hold the Trig Out high regardless of subsequent changes in the signal amplitude. If the latching mode is not enabled, the Trig Out will go from low to high, back to low, etc. depending on changes in the signal amplitude compared to the programmed threshold.

Veto: Data acquisition may be started with the trigger vetoed (disabled) to avoid premature triggering. A subsequent VME command will enable the trigger system.

SNAPSHOT FIFO

There are 1k sample programmable length, synchronized parallel load data FIFOs for each channel. All FIFOs in a system can be triggered in parallel for a snapshot in time. This allows phase synchronous, near real-time monitoring for off-board processing. FIFO operates independently of data storage to DRAM.

DATA READOUT

There are 2 readout modes

- 1 Direct DRAM readout one channel at a time** via VXI 16-bit data register.
- 2 Direct DRAM readout two channels at a time** via VXI 32-bit data register.

MEMORY

Size: 16M samples per channel.

Dual Port/Time Sliced Memory Access: Memory used as 16M FIFO for extended run applications.